Amendments to Drawings:

The attached sheet of drawings (6/6) includes changes to original Figure 6. This sheet replaces the original sheet (6/6) including Figures 6-8.

In Figure 6, the input to adder 610 has been changed from "I" to --Q-- and the output from adder 605 has been changed from "Q" to --I--.

REMARKS/ARGUMENTS

Claims 1, 2, 4, 6-8, 10-15, 17, 19-21, 23-26, 34, 36-38 and 40-49 are currently pending in this application. Claims 9, 22, 39 and 50-56 are cancelled without prejudice. Claims 1, 10, 14, 23, 34, 40 and 44-49 have been amended to more distinctly claim subject matter which the Applicants regard as the invention. A replacement sheet is submitted herewith to correct minor typographical errors found in Figure 6. The Applicants submit that no new matter has been added to the application by the amendments.

Telephonic Interview

The Examiner is thanked for granting a telephonic interview with the Applicants' representative on March 2, 2006. During the interview, the Examiner agreed that the claims would be patentable over Mohindra et al. (U.S. Patent No. 6,169,463) if further amended to recite that the first and second DC offset compensation values are determined by interpolating the minimum detected power readings associated with each of the signal inputs.

Claim Rejections

Claims 44-49 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,169,463 (Mohindra et al.). Mohindra discloses a quadrature modulator with set-and-forget carrier leakage compensation.

The Examiner is respectfully directed to refer to Figures 1, 2 and 6 of the Applicants' application. In accordance with the present invention, a digital direct current (DC) offset compensation module 210 (see Figure 2) is incorporated in a digital baseband (DBB) compensation processor 130 of a DBB transmitter 100 (see Figure 1) to correct, (i.e., suppress), carrier leakage associated with a modulator 170 in an analog radio transmitter 150 by adjusting the DC levels of in-phase (I) and

quadrature (Q) signal components 110, 115 based on previously determined (i.e., stored) first and second DC offset compensation values. A power detector 175 is used to determine respective first and second minimum detected power readings at the local oscillator (LO) frequency of the modulator 170.

First and second DC offset compensation values (i.e., compensation factors K_1 and K_2) are derived by interpolating the first and second minimum detected power readings. The first and second DC offset compensation values are then stored for future reference, whereby the DC levels of the I and Q signal components are adjusted based on the first and second DC offset compensation values, respectively.

Claims 44, 46 and 48 recite a digital DC offset compensation module having two signal inputs including an I signal component and a Q signal component, wherein a minimum detected power reading associated with each of the signal inputs is determined, first and second DC offset compensation values are determined by interpolating the minimum detected power readings, and the digital DC offset compensation module is configured to eliminate carrier leakage associated with the modulator by adjusting the respective DC levels of the two signal inputs based on the first and second DC offset compensation values.

Mohindra fails to teach or suggest determining a minimum detected power reading associated with each of the signal inputs. Furthermore, Mohindra fails to teach or suggest determining first and second DC offset compensation values by interpolating the minimum detected power readings. Additionally, Mohindra fails to teach or suggest a digital DC offset compensation module which is configured to eliminate carrier leakage associated with the modulator by adjusting the respective DC levels of the two signal inputs based on the first and second DC offset compensation values which are determined by interpolating the minimum detected power readings.

The Examiner asserts that the following portion (col. 2, lines 7-42) of Mohindra teaches the above-mentioned features:

> *"carrier leakage measurement means for measuring a first carrier leakage signal of said first local oscillator signal in said in-phase modulation branch, and a second carrier leakage signal of said second local oscillator signal in said quadrature branch;*
>
> *a controllable signal generating means for generating a first monotonously increasing signal and a second monotonously increasing signal; and*
>
> *holding means for holding values of said first and second monotonously increasing signals, said holding means being coupled to said first and second summing means so as to form feedback paths;*
>
> *said carrier leakage measurement means adopting a first state in which said first and second carrier leakage signals are measured, and a second state in which said controllable signal generating means is controlled to stop generating said first and second monotonously increasing signals, said second state being adopted from said first state during measurement of said first and second carrier leakage signals.*
>
> *The invention is based upon the insight that usually parameters influencing carrier leakage are slowly varying with time so that there is no need for continuous compensation. Based upon this insight, it was realized that a simple but robust carrier leakage compensation could be implemented being operative at predetermined points in time, such at switching on power, or, when used in a communications apparatus, possibly also at channel switching. When used in a communication device such as a broad band CDMA communications device, in which, in principle, no channel switching is needed, there is only a needed to apply carrier leakage compensation at power on of the communications device. In such a case, after power on, power to components used for carrier leakage compensation could even be switched off, thus achieving power savings in such a portable communications device."*

The Applicants submit that nowhere in the portion of Mohindra presented above is the feature of determining a minimum detected power reading associated with each of the signal inputs taught or suggested. Furthermore, nowhere in the

portion of Mohindra presented above is the feature of determining first and second DC offset compensation values by interpolating the minimum detected power readings taught or suggested. Additionally, nowhere in the portion of Mohindra presented above is the feature of a digital DC offset compensation module which is configured to eliminate carrier leakage associated with the modulator by adjusting the respective DC levels of the two signal inputs based on the first and second DC offset compensation values which are determined by interpolating the minimum detected power readings taught or suggested.

Since Mohindra fails to disclose all of the features recited in claims 44, 46 and 48, the Applicants submit that claims 44, 46 and 48 are patentable over the prior art of record.

With respect to claims 45, 47 and 49, these claims are dependent upon claims 44, 46 and 48, respectively, and are believed to be allowable for the same reasons provided above.

In view of the arguments presented above, the withdrawal of the rejection of claims 44-49 under 35 U.S.C. §102(b) is respectfully requested.

Claims 1, 2, 7, 8, 14, 15, 20, 21, 34, 37 and 38 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0219884 (Mo et al.) in view of U.S. Patent No. 6,759,902 (Kossor).

The independent claims 1, 14 and 34 have been amended to incorporate the subject matter of dependent claims 1, 22 and 39.

Claims 9, 10, 22, 23, 39 and 40 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mo and Kossor, and further in view of Mohindra. The features of claims 9, 22 and 39 are the same as the features described above with respect to claims 44, 46 and 48, and the Examiner relies on the same portion of Mohindra to reject claims 9, 22 and 39.

As already mentioned above, the Applicants submit that nowhere in the portion of Mohindra presented above is the feature of determining a minimum detected power reading associated with each of the signal inputs taught or suggested. Furthermore, nowhere in the portion of Mohindra presented above is the feature of determining first and second DC offset compensation values by interpolating the minimum detected power readings taught or suggested. Additionally, nowhere in the portion of Mohindra presented above is the feature of a digital DC offset compensation module which is configured to eliminate carrier leakage associated with the modulator by adjusting the respective DC levels of the two signal inputs based on the first and second DC offset compensation values which are determined by interpolating the minimum detected power readings taught or suggested.

Since Mohindra fails to disclose all of the features recited in amended claims 1, 14 and 34, the Applicants submit that claims 1, 14 and 34 are patentable over the prior art of record.

With respect to claims 2, 4, 6-8, 10-13, 15, 17, 19-21, 23-26, 36-38 and 40-43, these claims are dependent upon claims 1, 14 and 34, respectively, and are believed to be allowable for the same reasons provided above.

In view of the arguments presented above, the Applicants submit that claims 1, 2, 4, 6-8, 10-15, 17, 19-21, 23-26, 34, 36-38 and 40-43 are patentable over the prior art of record.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1, 2, 4, 6-8, 10-15, 17, 19-21, 23-26, 34, 36-38 and 40-49, is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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Enclosures